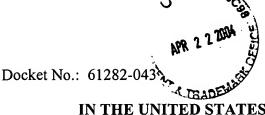
PATENT



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Customer Number: 20277

Takuya KOBAYASHI

Confirmation Number: 1414

Serial No.: 10/698,532

Group Art Unit: 2858

Filed: November 03, 2003

Examiner: Unknown

For:

PATH DELAY MEASURING CIRCUITRY

INFORMATION DISCLOSURE STATEMENT

Mail Stop IDS Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

The relevance of the article, "Delay Fault Testing for VLSI Circuits" is discussed in the present specification.

10/698,532

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Michael E. Fogarty. Registration No. 36,139

600 13th Street, N.W. Washington, DC 20005-3096 (202) 756-8000 MEF:tlb Facsimile: (202) 756-8087

Date: April 22, 2004

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION									ERIAL NO. 0/698,532			
MR 22 2004 2 (PTO-1449)						APPLICANT Takuya KOBAYASHI						
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Angela KRSTIC, et al., "Delay Fault Testing for VLSI Circuits", pp. 7-12, Kluwer Academic Publishers, 1998.												
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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.